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EXAMINER	
WILLIAMS, LAWRENCE B	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/903,306	LU, GUANGMING	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed. Examiner suggests applicant submit new drawings for Figs. 8-11, 13-15 with larger lettering.

2. Figures 1-4 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because line 13 is unclear beginning with "for configuring...". Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities: Examiner suggests applicant define the acronym BCJR in paragraph [0009].

Appropriate correction is required.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claim 10 is objected to because of the following informalities: Examiner suggest applicant insert "**of**" between portion and **the** in line 8 of the claim.. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

8. Claims 1-5, 9-12, 14-17, 20 are rejected under 35 U.S.C. 102(a) as being anticipated by Saunders (US Patent 6,175,940 B1).

(1) With regard to claim 1, Saunders discloses in Fig(s). 2-6, discloses a digital signal processing method, comprising: configuring a portion of an array of independently reconfigurable processing elements for performing a turbo coding routine (col. 2, lines 31-35); and executing the turbo coding routine on data blocks received at the configured portion of the array of processing elements (col. 3, lines 32-39; col. 4, lines 36-46).

(2) With regard to claim 2, claim 2 inherits all limitations of claim 1 above. Furthermore, Saunders also discloses in Fig. 5, wherein configuring a portion of the array of reconfigurable processing elements includes activating the portion with an activation signal (signal from programmer controller (30)).

(3) With regard to claim 3, claim 3 inherits all limitations of claim 1 above. Furthermore, Saunders discloses in Fig. 5, wherein the portion of the array of independently reconfigurable processing elements includes at least one processing element (62).

(4) With regard to claim 4, claim 4 inherits all limitations of claim 1 above. Furthermore, Saunders discloses in Fig. 5, wherein executing the turbo coding routine on data blocks received at the configured portion of the array of processing elements includes encoding (42, 62) the data blocks.

(5) With regard to claim 5, claim 5 inherits all limitations of claim 1 above. Furthermore, Saunders discloses wherein executing the turbo coding routine on data blocks received at the configured portion of the array of processing elements includes decoding the data blocks (col. 2, lines 35-38).

(6) With regard to claim 9, claim 9 inherits all limitations of claim 1 above. Furthermore, Saunders discloses wherein each processing element includes at least one functional unit, and wherein configuring a portion of an array of independently reconfigurable processing elements for performing a turbo coding routine includes programming the functional unit to perform at least one function of the turbo coding routine (col. 3, lines 32-50).

(7) With regard to claim 10, claim 10 inherits all limitations of claim 9 above. Furthermore, Saunders also discloses wherein the function unit includes programmable logic that is configurable for performing a logical function (col. 3, lines 43-50).

(8) With regard to claim 11, Saunders discloses in Fig. 5, a digital signal processing apparatus, comprising: an array of interconnected, reconfigurable processing elements (24), each processing element being independently programmable with a context instruction; a context memory (30) connected to the array for storing and providing the context instruction to the processing elements; and a processor connected to the array and to the context memory, for controlling the loading of the context instruction to the processing elements, for configuring a portion the processing elements to perform a turbo coding routine (col. 3, lines 43-50). The programmer controller acts a memory for storing and providing context instruction and also control the loading of the instructions for configuring the filed programmable logic array(s) 24).

(9) With regard to claim 12, Saunders also discloses wherein the processor is further configured to execute the turbo coding routine by controlling a state of the configured portion of processing elements (col. 3, lines 42-50).

(9) With regard to claim 14, claim 14 inherits all limitations of claim 11 above. Furthermore, Saunders also discloses in Fig. 5, wherein the turbo coding routine is an encoding process on data blocks received at the portion of the array (col. 2, lines 31-35).

(10) With regard to claim 15, claim 15 inherits all limitations of claim 11 above. Furthermore, Saunders also discloses in Fig. 6, wherein the turbo coding routine is a decoding process on data blocks received at the portion of the array (col. 2, lines 35-28).

(11) With regard to claim 16, Saunders also discloses wherein each processing element

includes at least one functional unit that is programmable for performing at least one function of the turbo coding routine (col. 3, lines 28-41).

(12) With regard to claim 17, Saunders also discloses wherein the function unit includes programmable logic that is configurable by the context instruction. (col. 3, lines 43-50).

(13) With regard to claim 20, Saunders discloses in Fig. 5, a digital signal processing apparatus, comprising: a context memory (30) for storing one or more context instructions for performing a turbo coding routine; and an array of independently reconfigurable processing elements, each of which is responsive to a context instruction for being configured to execute a portion of the turbo coding routine. The programmer controller acts a memory for storing and providing context instruction and also control the loading of the instructions for configuring the filed programmable logic array(s) 24) (col. 2, lines 31-35; col. 3, lines 32-39; col. 4, lines 36-46).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 6, 7, 13, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders U.S. Patent 6,175,940 B1 as applied to claims 1 and 11 above, and further in view of Nguyen U.S. Patent 6,813,742 B2).

(1) With regard to claim 6, as noted above Saunders discloses all limitations of claim 1

above. Saunders does not however teach configuring the portion as a logarithmic maximum a posteriori (LOG-MAP) -based processor.

However, Nguyen teaches a logarithmic maximum a posteriori (LOG-MAP) -based processor (claim 3).

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Nguyen to modify the invention of Saunders because it is well known in the art that Maximum a posteriori (MAP) based methods have proven to be the best for implementing iterative decoding of turbo codes.

(2) With regard to claim 7, claim 7 inherits all limitations of claim 6 above. Furthermore, Nguyen also discloses the method further comprising configuring the portion to access a look-up table (col. 8, line 61-col. 9, line 4).

(3) With regard to claim 13, Nguyen discloses his processor subsystem implemented in an ASIC (application-specific-integrated-circuit) of an SoC (system-on-chip) device, or in an VLSI (very large-scale integrated circuits) device for wireless communication applications.

(4) With regard to claim 19, claim 19 inherits all limitations of claims 11 and 6 above.

11. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders U.S. Patent 6,175,940 B1 as applied to claims 1 and 11 above, and further in view of Stephen et al. US Patent 6,484,283 B2.

(1) With regard to claim 8, as noted above Saunders discloses all limitations of claim 1 above. Saunders does not however disclose idling all processing elements in the array other than the portion of processing elements configured for performing the turbo coding routine.

However, Stephen et al. discloses an idling state in his invention of encoding and decoding a turbo code as a measure of power consumption (col. 31, lines 4-23).

Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to apply the method as taught by Stephen et al. to modify the invention of Saunders simply as a measure of power consumption.

(2) With regard to claim 18, claim 18 inherits all limitations of claims 11 and 8 above.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Rhee et al. discloses in U.S. Patent 6,807,231 B1 a Method And Apparatus For Decoding M-PSK Turbo Code Using New Approximation Technique.

b.) Hladik et al. discloses in U.S. Patent 5,721,745 Parallel Concatenated Tail-Biting Convolutional Code And Decoder Therefor.

c.) Le Bars et al. discloses in U.S. 2002/0041640 A1 a Method And Device For Evaluating The Noise Associated With TurboCodes, And Systems Using Them.

d.) Coombs et al. discloses in U.S. Patent 6,718,504 B1 a Method and Apparatus For Implementing A Data Processor Adapted For Turbo Decoding.

e.) Coombs et al. discloses in U.S. 2004/0225949 A1 a Method and Apparatus For Implementing A Data Processor Adapted For Turbo Decoding.

f.) Smith et al. discloses in U.S. 2004/0005019 A1 Turbo Decoder Employing Max And Max* Map Decoding.

g.) Worm et al. discloses in U.S. 2003/0002603 A1 a Method And Apparatus For Decoding A Bit Sequence.

h.) Crozier et al. discloses in U.S. Patent 6,145,114 a Method And Enhanced Max-Log-A Posterior Probability Processing.

g.) Worm et al. discloses in U.S. 2003/0002603 A1 a Method And Apparatus For Decoding A Bit Sequence.

h.) Crozier et al. discloses in U.S. Patent 6,145,114 a Method And Enhanced Max-Log-A Posterior Probability Processing.

i.) Ishikawa discloses in U.S. Patent 6,523,146 B1 Operation Processing Apparatus And Operation Processing Method.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
December 13, 2004

Amandale

AMANDA T. LE
PRIMARY EXAMINER